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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Patent Application Serial No. .... 10/733,181  
Filing Date ..... December 10, 2003  
Inventor ..... H. Montgomery Manning et al.  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2812  
Examiner ..... Unknown  
Attorney Docket No. .... MI22-2295  
Customer No. .... 021567  
Title: Semiconductor Constructions, and Methods of Forming Capacitor Devices

Assistant Commissioner for Patents  
P.O. Box 1450  
Alexandria VA 22313-1450

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2. Supplemental Information Disclosure Statement with Form PTO-1449
3. Cited References (3)

Dated: 4/19/05By: 

Natalie King

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NUMBER OF PAGES IN FACSIMILE: 19

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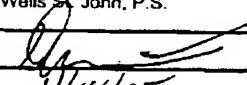
PTO/SB/21 (03-03)

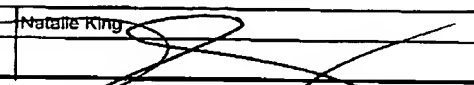
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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	10/733,181
	Filing Date	12/10/2003
	First Named Inventor	Manning et al.
	Art Unit	2834
	Examiner Name	Unknown
	Attorney Docket Number	MI22-2295
Total Number of Pages in This Submission		

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual	David G. Latwesen, Ph.D., Reg. No. 38,533 Wells St. John, P.S.
Signature	
Date	4/18/05

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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References -- See Attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing of a first Office Action on the merits, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: 4/18/05By: David G. Latwesen, Ph.D.  
Reg. No. 38,533

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	APPLICANT: H. Montgomery Manning et al.	
	FILING DATE December 10, 2003	GROUP 2834

U.S. PATENT DOCUMENTS							
Examine's Initials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	AA	6,204,143	3/2001	Roberts et al.			
	AB	6,180,450	1/2001	Dennison			
	AC	5,340,763	8/1994	Dennison			
	AD	6,403,442	6/2002	Reinberg			
	AE	6,037,218	3/2000	Dennison et al.			
	AF	5,652,164	7/1997	Dennison et al.			
	AG	5,498,562	12/1996	Dennison et al.			
	AH	5,401,681	3/1995	Dennison et al.			
	AI	5,605,857	2/1997	Jost et al.			

FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AJ	DE 4447804 C2	1/24/2002	Germany (Abstract)				X
	AK							
	AL							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
	AM	PCT/US2004/027898; Filed: 8/26/2004; PCT Search Report mailed 2/28/2005; 4 pp.
	AN	"Novel Robust Cell Capacitor (Leaning Exterminated Ring Type Insulator) And New Storage Node Contact (Top Spacer Contact) For 70nm DRAM Technology And Beyond"; Park et al.;
		2004 Symposium on VLSI Technology Digest of Technical Papers; 7/2004; pp. 34-35.
EXAMINER		DATE CONSIDERED
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U.S. PATENT DOCUMENTS							
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,705,838	1/1998	Jost et al.			
	AB	5,686,747	11/1997	Jost et al.			
	AC	5,702,990	12/1997	Jost et al.			
	AD	5,821,140	10/1998	Jost et al.			
	AE	5,900,660	5/1999	Jost et al.			
	AF	6,110,774	8/2000	Jost et al.			
	AG	2002-086479	7/2002	Reinberg			
	AH	2002-090779	7/2002	Jang			
	AI	2002-163026	11/2002	Park			
	AJ	2001-026974	10/2001	Reinberg			
	AK	2002-039826	4/2002	Reinberg			

FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
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